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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,415	01/15/2004	Hisashi Kaneko	04173.0441	3384
22852 7590 05/22/2007 FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP 901 NEW YORK AVENUE, NW WASHINGTON, DC 20001-4413			EXAMINER SHARON, AYAL I	
			ART UNIT 2123	PAPER NUMBER
			MAIL DATE 05/22/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/757,415	Applicant(s) KANEKO ET AL.	
	Examiner Ayal I. Sharon	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 March 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5,8-10,13-15 and 18-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 8-10,13-15 and 18-20 is/are allowed.
- 6) ☒ Claim(s) 1 and 3-5 is/are rejected.
- 7) ☒ Claim(s) 2 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 June 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Introduction

1. Claims 1-5, 8-10, 13-15, and 18-20 of U.S. Application 10/757,415 filed on 1/15/2004 are currently pending.
2. The application claims benefit of Japanese Application P2003-344526, filed on 10/2/2003.

Drawings

3. Figure 2 is objected to because the phrase "and so forth" is vague and ambiguous. The Applicants have relied on Fig.2 in order to overcome 35 U.S.C. § 112, first paragraph rejections, therefore, the scope of the disclosure in Fig.2 must be definite in order to avoid 35 U.S.C. § 112, second paragraph rejections.
4. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief

description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

6. The prior art used for these rejections is as follows:

a. Kameda, Y. and S. Yoroazu. "Automatic Josephson-Transmission-Line Routing for Single-Flux-Quantum Cell-Based Logic Units." IEEE Transactions on Applied Superconductivity. June 2003. Vol.13, Issue 2, pp. 519-522. ("**Kameda**").

7. **Claims 1, and 3-4 are rejected under 35 U.S.C. 102(a) as being anticipated by Kameda.**

8. In regards to Claim 1, Kameda teaches the following limitations:

1. A simulation circuit pattern evaluation method, comprising:

designing an aggregate of simulation circuit patterns,

(See Kameda, especially: Sections III(B) and III(C), and Figures 5 and 7)

which simulate a circuit pattern of a semiconductor integrated circuit,

(See Kameda, especially: Sections III(B) and III(C), and Figures 5 and 7)

by combining plural geometrical structure defining parameters including at least any one of a dummy wiring group formation position and an existence of dummy via hole,

(See Kameda, especially: Sections III(B) and III(C), and Figures 5 and 7)

the plural geometrical structure defining parameters respectively having at least two states,

(See Kameda, especially: Section IV(B), which teaches a "bar" state and a "cross" state)

in such a manner that the respective states appear the same number of times in the respective geometrical structure defining parameters;

(See Kameda, especially: Section IV(B), which teaches a "bar" state and a "cross" state)

forming the aggregate of simulation circuit patterns on a substrate;

(See Kameda, especially: Sections IV(B) and IV(C))

and evaluating the formed aggregate of the simulation circuit patterns.

(See Kameda, especially: Sections IV(B) and IV(C))

9. In regards to Claim 3, Kameda teaches the following limitations:

3. The simulation circuit pattern evaluation method as set forth in claim 1,

wherein said forming is performed with a predetermined process condition; and

wherein said evaluating includes evaluating a suitability of a circuit pattern of a semiconductor integrated circuit for the predetermined process condition based on the aggregate of the simulation circuit patterns.

(See Kameda, especially: Sections IV(B) and IV(C))

10. In regards to Claim 4, Kameda teaches the following limitations:

*4. The simulation circuit pattern evaluation method as set forth in claim 1,
wherein the geometrical structure defining parameters are parameters which define a geometrical structure of a wiring.*

(See Kameda, especially: Sections III(B) and III(C), and Figures 5 and 7)

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35

U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35

U.S.C. 103(a).

13. The prior art used for these rejections is as follows:

- a. Kameda, Y. and S. Yorozu. "Automatic Josephson-Transmission-Line Routing for Single-Flux-Quantum Cell-Based Logic Units." IEEE Transactions on Applied Superconductivity. June 2003. Vol.13, Issue 2, pp. 519-522. ("**Kameda**").
- b. Muddu, S. et al. "Repeater and Interconnect Strategies for High-Performance Physical Designs." Proc. XI Brazilian Symposium on IC Design. Sept.30 – Oct.3, 1998. pp.226-231. ("**Muddu**").

14. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

15. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kameda in view of Muddu.

16. In regards to Claim 5, Kameda does not expressly teach the claimed limitations:

*5. The simulation circuit pattern evaluation method as set forth in claim 4,
wherein the parameters which define the geometrical structure of the wiring further include at least any one of a wiring formation width, a wiring formation length, a via hole formation position, and a wiring group formation length.*

Muddu, on the other hand, expressly teaches the wire width and spacing parameters defined in Table 5, in "2.5. Effect of Interconnect Slew Time", and in "3. Effects of Shield Wiring. Examiner notes that the parameters in Table 1 of the instant application include "wiring formation width" and "wiring formation height".

Kameda and Muddu are analogous art because they are from the phrase same field of endeavor.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify Kameda to include the wiring info taught in Muddu.

The suggestion/motivation for combining the references would have been Kameda's description of wiring characteristics in Sections III(B) and III(C).

Therefore, it would have been obvious to a person of ordinary skill in the art to modify Kameda with Muddu to obtain the invention as specified in Claim 5.

Allowable Subject Matter

17. Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Kameda does not expressly teach the limitations recited in claim 2:

2. The simulation circuit pattern evaluation method as set forth in claim 1,

wherein said forming includes forming the aggregate of the simulation circuit patterns on each of a plurality of the substrates with a process condition which is different for each of the substrates; and

wherein said evaluating includes separately evaluating the aggregate of the simulation circuit patterns on each of the substrates.

18. Claims 8-10, 13-15, and 18-20 are allowed.

Art Unit: 2123

19. The following is an examiner's statement of reasons for allowance for claims 8-10, 13-15, and 18-20.

20. In regards to Claim 8, Kameda teaches the following limitations:

8. A manufacturing method of a semiconductor integrated circuit, comprising:

designing an aggregate of simulation circuit patterns,

(See Kameda, especially: Sections III(B) and III(C), and Figures 5 and 7)

which simulate a circuit pattern of a semiconductor integrated circuit,

(See Kameda, especially: Sections III(B) and III(C), and Figures 5 and 7)

by combining plural geometrical structure defining parameters including at least any one of a dummy wiring group formation position and an existence of dummy via hole,

(See Kameda, especially: Sections III(B) and III(C), and Figures 5 and 7)

the plural geometrical structure defining parameters respectively having at least two states,

(See Kameda, especially: Section IV(B), which teaches a "bar" state and a "cross" state)

in such a manner that the respective states appear the same number of times in the respective geometrical structure defining parameters;

(See Kameda, especially: Section IV(B), which teaches a "bar" state and a "cross" state)

... and forming the circuit pattern with the detected process condition.

(See Kameda, especially: Sections IV(B) and IV(C))

Kameda, however, does not expressly teach the following limitations:

forming the aggregate of the simulation circuit patterns on each of plural substrates with a process condition which is different for each of the substrate;

detecting a process condition which is suitable for the aggregate of the simulation circuit patterns by separately evaluating the formed aggregate of the simulation circuit patterns on each of the substrate;

21. Dependent claims 9-10 are allowable because independent claim 8 is allowable.

22. Claims 13-15 and 18-20 are allowable for the same reasons as claims 8-10.

Claims 13-15 are apparatus ("substrate") claims, and claims 18-20 are apparatus ("substrate group") claims that recite limitations equivalent to those recited in method claims 8-10 and taught throughout Kameda and Muddu.

Response to Arguments

Claim Rejections - 35 USC § 112

23. Examiner finds Applicants' arguments filed 3/19/07 to be persuasive. The 35 USC § 112 rejections have been withdrawn.

Claim Rejections - 35 USC § 102(b)

24. Examiner has withdrawn the 35 U.S.C. § 102(b) rejections based on the Muddu reference in light of Applicants' claim amendments. Since the amendments did not roll-up dependent claims, but rather incorporated selected elements into the independent claims, the new claims have a scope that was not previously presented.

25. New art rejections have been applied.

Conclusion

26. The following prior art, made of record and not relied upon, is considered pertinent to applicant's disclosure.

27. U.S. Patent 6,253,362 to Anand et al. (Examiner notes that in col.1, lines 47-56, Anand teaches that positioning via holes was old and well known in the art).

28. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a bi-week, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753.

Any response to this office action should be faxed to (571) 273-8300, or mailed to:

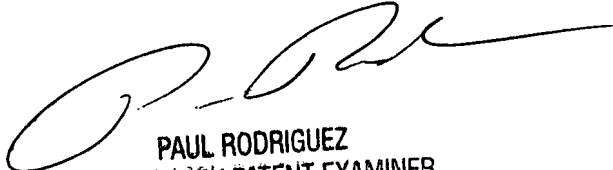
USPTO
P.O. Box 1450
Alexandria, VA 22313-1450

or hand carried to:

USPTO
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (571) 272-2100.

Ayal I. Sharon
Art Unit 2123
May 17, 2007


PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100